Amendments to the Claims:

1. (Currently Amended) A method for forming a floating gate memory array comprising:

forming a gate dielectric layer on a substrate, wherein the substrate extends horizontally in perpendicular X and Y directions;

forming a floating gate material layer on the gate dielectric layer;

forming a disposable material layer on the floating gate material layer;

etching column strips in the Y direction through the disposable material layer, floating gate material layer and the gate dielectric layer to form isolation trenches into the substrate which extend longitudinally in the Y direction;

forming an insulator material to a vertical height above the disposable material layer;

planarizing the insulator material to expose a top region of the disposable material layer;

removing the disposable material layer to expose a top region of the floating gate material layer, wherein the top region of the floating gate material layer is recessed below a top surface of the planarized insulator material;

forming layers of an intermediate dielectric, a conductive wordline, a tungsten silicide and an insulation cap;

etching row strips in the X <u>direction</u> through the floating gate material layer to a depth of at least the gate dielectric layer to define transistor gates;

performing a source implant to form rows of source regions in the substrate extending in the X direction in alternate ones of the row strips;

performing a source/drain implant to simultaneously form drain regions unique to a respective transistor while increasing a doping of the rows of source regions;

forming dielectric transistor gate spacers;

forming a conformal etch stop barrier layer over the transistor gates, the gate spacers, the source regions and the drain regions;

forming a planarized insulation material over the etch stop barrier layer;

performing a via etch through the planarized insulation material to completely clear the planarized insulation material residing between the transistor gates, thus exposing ~~expose~~ the etch stop barrier layer and forming rows of source line vias running in the X direction and separate drain vias unique to each transistor running in the Y direction; ~~and~~

clearing a horizontal component of the conformal etch stop barrier layer that covers the source regions and drain regions; and

forming individual drain contacts to a respective transistor gate and rows of source contact interconnects, wherein the individual drain contacts and the rows of source contact interconnects substantially fill openings between the transistor gates and abut to a vertical component of the conformal etch stop barrier layer residing on the transistor gates.

2. (Currently Amended) A method of forming floating gate transistors comprising:

etching isolation trenches in a Y direction through a layer of floating gate material and tunneling dielectric, wherein the isolation trenches vertically extend into an underlying substrate;

forming an intermediate dielectric layer and a tungsten comprising control gate material layer on the floating gate material;

etching the control gate, intermediate dielectric layer, and the floating gate material in an X direction, wherein X is perpendicular to Y, to form individual floating gates from the floating gate material that have defined boundaries in the X and Y directions for individual floating gate transistors, and to form word lines from the control gate material having a defined width in the Y direction and extending in the X direction such that multiple transistors spaced apart in the X direction share a common word line;

implanting common source regions extending in the X direction such that multiple transistors spaced apart in the X direction share a common source region;

implanting drain regions such that transistors spaced apart in the X direction do not share a common drain region;

<u>forming a conformal etch stop barrier layer over the control gates of the common source regions and the drain regions;</u>

<u>forming a planarized insulation material over the conformal etch stop layer;</u>

performing a via etch through the planarized insulation material to completely clear the planarized insulation material residing between the control gates and exposing the etch stop barrier layer thereunder;

clearing a horizontal component of the conformal etch stop barrier layer from the source regions and drain regions; and

forming rows of source line contacts running in the X direction to form an electrical connection to the common source regions; and

forming individual drain contacts to the drain regions;

wherein the rows of source line contacts and the individual drain contacts substantially fill openings between the control gates and abut to a vertical component of the conformal etch stop barrier layer residing on the control gates.

3. (Currently Amended) A method for forming a flash memory device in a semiconductor assembly, comprising:

forming an oxide layer, a polysilicon layer and a nitride layer on a silicon substrate;

patterning to define active areas and columns of trenches running in a y-direction of the silicon substrate;

etching the nitride layer, the polysilicon layer and the oxide layer to form the columns of trenches therein and to define gates locations thereunder;

forming oxide to fill the columns of trenches and cover the patterned nitride layer;

planarizing the oxide to form columns of trench isolation running in the y-direction and exposing the patterned nitride layer;

removing the patterned nitride layer to expose the patterned polysilicon layer;

forming transistor gates running in an x-direction of the silicon substrate, the transistor gates comprising the patterned oxide, the patterned polysilicon layer, a tunnel oxide, a floating gate, an inter-polysilicon dielectric, a polysilicon wordline, a tungsten silicide and an insulation cap;

etching portions of the trench isolation to form rows of exposed silicon substrate running in the x-direction;

implanting to form rows of source regions self-aligned to the transistor gates, each source region in a common row being connected together;

implanting to simultaneously form separate drain regions unique to a respective transistor while doping the source regions;

forming dielectric spacers on the transistor gates;

forming a <u>conformal</u> barrier layer over the transistor gates, the dielectric spacers, the source regions and drain regions;

forming a planarized insulation material over the barrier layer;

<u>performing a via etch through the planarized insulation material to completely clear the planarized insulation material residing between the transistor gates lined with the conformal barrier layer,</u>

etching to expose an underlying <u>conformal</u> barrier layer and to simultaneously form rows of source line vias running in the x-direction and separate drain vias unique to each transistor;

etching to remove <u>a horizontal component of</u> the exposed underlying barrier layer from the surface of the source regions and drain regions;

forming a titanium nitride layer into the source and drain vias to make contact with the source regions and drain regions <u>such that the titanium nitride layer abuts to a vertical component of the conformal barrier layer lining the transistor gates</u>;

forming a tungsten-based metal into the source and drain vias thus making contact with the titanium nitride layer; and

planarizing the tungsten-based metal and the titanium nitride layer to simultaneously form individual drain contacts self-aligned to a respective transistor gate and rows of source interconnects, each row of source interconnects running a major length and major width of a respective underlying row of commonly connected source regions and making substantially continuous contact therebetween.

4. (Original) The method of claim 3, wherein said tungsten-based metal comprises titanium/tungsten.

5. (Currently Amended) A method for forming a flash memory device in a semiconductor assembly, comprising:

on a silicon substrate and along a y-axis thereof, forming device isolation separated by material to define gate locations thereunder;

forming transistor gates at the gate locations;

removing the device isolation to expose the underlying silicon substrate at source locations running along an x-axis of the silicon substrate, the removal of the device isolation forming source locations self-aligned to the transistor gates;

implanting into the exposed underlying silicon substrate to form source regions self-aligned to the transistor gates and commonly connected together in a row along the x-axis;

implanting to simultaneously form drain regions while increasing the doping of the source regions;

forming a conformal dielectric material over the transistor gates, the source regions and the drain regions;

forming a planarized insulation material over the conformal dielectric layer;

performing a via etch through the planarized insulation material to completely clear the planarized insulation material residing between the transistor gates lined with the conformal dielectric material,

forming source and drain openings in the by clearing a horizontal component of the conformal dielectric material ~~that~~ to expose the source regions and the drain regions;

forming metal into the source and drain via openings to make contact with the source regions and the drain regions such that the metal substantially fills the via openings and abuts to a vertical component of the conformal dielectric material lining the transistor gates; and

planarizing the metal to simultaneously form individual drain contacts self-aligned to a respective transistor gate and a row of source interconnects, each row of source interconnects running a major length and major width of a respective underlying row of commonly connected together source regions and making substantially continuous contact therebetween.

6. (Original) The method of claim 5, wherein said tungsten-based metal comprises titanium/tungsten.